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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448

7590 06/16/2004

ON Semiconductor
Patent Administration Dept - MD A700
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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,145	AVERETT ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,and26-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In both claims, the limitation, "*wherein a wall of the second recessed region is substantially absent second dielectric material,*" is vague and indefinite. From Webster's Dictionary, the definition of "absent" is "not present." Hence, "substantially absent" would read as "less than totally not present," which is difficult to interpret as a limitation. Examiner will assume that Applicant meant to recite that a portion of the second material is present on the wall of the second recess.

Claim Rejections – 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5, 6, 8 – 11, and 26 – 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al. '041 (US 5,640,041).

5. Regarding Claim 1, Lur et al. disclose a semiconductor device formed in a monocrystalline silicon substrate (Col. 3, line 67) where a second recessed region (22) (See Figure 6) is formed within a first recessed region (15,16) etched from a deposited silicon dioxide layer (Col. 4, lines 53 - 55) and the surface of trenches covered with silicon dioxide (CVD) (cap layer) to seal the "voids" or trenches (Col. 3, lines 10 – 15). The walls of trenches are covered with silicon dioxide (25) (See Figure 10).
Lur et al. '041 do not disclose that the second dielectric material (SiO2) is thermally grown. However, for this application, the device of Lur et al. prepared by using a CVD sealing layer is the same as that recited in the instant application, wherein the device is produced as a product-by-process. The court has ruled that "*determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art was made by a different process.*" In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

6. Regarding Claim 2, Lur et al. disclose that an active device is formed in an active region (See Figure 14) with a gate dielectric (4), gate electrode (5), and doped regions (52,54) (n+,n-) at the peripheral edges.

7. Regarding Claim 5, Lur et al. disclose (Col. 3, line 67) that the substrate is silicon.

8. Regarding Claim 6, Lur et al. disclose (Col. 4, lines 1 – 4) that the dielectric material

is silicon dioxide.

9. Regarding Claim 8, as discussed previously, Lur et al. do not disclose that the second silicon dioxide layer is thermally grown, but rather formed by CVD. For this application, the device of Lur et al. prepared by using a CVD sealing layer is the same as that recited in the instant application, wherein the device is produced as a product-by-process. The court has ruled that "*determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art was made by a different process.*" In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

10. Regarding Claim 9, as discussed previously, Lur et al. disclose that the dielectric layer forms a cap layer.

11. Regarding Claim 10, Lur et al. disclose that the first dielectric layer is formed by CVD (Col. 4, lines 1 – 4).

12. Regarding Claim 11, Lur et al disclose that the depth of trenches in the second recessed region for the narrow trenches (17) (See Figure 6) is 20,000 Angstroms (2um) (Col. 4,lines 39 – 40),which is consistent with the depth recited in the instant application, subject to optimization for a particular device application.

13. Regarding Claim 26, Lur et al. disclose a semiconductor device formed in a

monocrystalline silicon substrate (Col. 3, line 67) where a second recessed region (22) (See Figure 6) is formed within a first recessed region (15,16) etched from a deposited dielectric material (12, Figure 5) with a semiconductor layer (14) overlying the dielectric layer. Further Lur et al. disclose that the surface of trenches is covered with silicon dioxide (CVD) (cap layer) to seal the created "voids" or trenches (Col. 3, lines 10 – 15) formed by a deposition shadowing effect (Wolf, p.197, Figure 4-8). The walls of trenches are covered with silicon dioxide (25) (See Figure 10) and the structure totally sealed. Lur et al. do not disclose that the second dielectric material (SiO2) is thermally grown. However, for this application, the device of Lur et al. prepared by using a CVD sealing layer is the same as that recited in the instant application, wherein the device is produced as a product-by-process. The court has ruled that "*determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior art was made by a different process.*" In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

14. Regarding Claim 27, Lur et al. disclose (14) (Figure 5) that the semiconductor layer is deposited polysilicon.

15. Regarding Claim 28, Lur et al. do not disclose that the second dielectric material is thermally grown silicon dioxide, but rather by CVD. As mentioned previously, for this application, a thermally grown and a CVD layer are functionally equivalent.

16. Regarding Claim 29, Lur et al. disclose that an active device is formed in an active region (See Figure 14) with a gate dielectric (4), gate electrode (5), and doped regions (52,54) (n+,n-) at the peripheral edges.

17. Claims 3, 4, 30, and 31 are rejected under 35 U.S.C. 103(a) as unpatentable over Lur et al. as applied to Claims 1, 2, 5, 6, 8 – 11, and 26 - 29 above, and further in view of Zekeriya et al. (US 2003/0030107 A1).

18. Regarding Claims 3 and 4, Lur et al. do not disclose the presence of a passive device or component formed over the second recessed region. However, Zekeriva et al. disclose the formation of a resistor (106) Figure 13) on a dielectric layer (104) with a metal plug (126") for electrical contact. Hence it would have been obvious at the time of the invention to one of ordinary skill in the art to use the technique of Zekeria et al. to form a resistor on the overlying dielectric layer in Lur et al. to obtain a component with reduced parasitic capacitance owing to the large volume of air pockets and low permittivity of the underlying region.

19. Regarding Claims 30 and 31, Lur et al. do not disclose the presence of a passive device or component formed over the second recessed region. However, Zekeriva et al. disclose the formation of a resistor (106) Figure 13) on a dielectric layer (104) with a metal plug (126") for electrical contact. Hence it would have been obvious at the time of the invention to one of ordinary skill in the art to use the technique of Zekeria et al. to form a resistor on the overlying dielectric layer in Lur et al. to obtain a component with reduced parasitic capaci-

tance owing to the large volume of air pockets and low permittivity of the underlying region.

20. Claims 7, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al.,as applied to Claims 1, 2, 5, 6, 8 – 11, and 26 – 29 above, and further in view of Holbrook et al. (US 6,495,853 B1).

21. Regarding Claim 7, Lur et al. do not disclose the presence of a third dielectric material deposited on the walls of trenches. However, it is routine to form a liner layer on the walls and Holbrook et al. disclose (422) (Figure 6) the formation of a silicon nitride layer (Col. 6, lines 63 67) on the walls of the trench. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Holbrook et al. with Lur et al. to provide a liner layer that would reduce sharp edges and roughness of subsequent deposited layers (Col. 6, lines 63 – 67).

22. Regarding Claims 32 and 33, Lur et al. do not disclose the presence of a third dielectric material deposited on the walls of trenches. However, it is routine to form a liner layer on the walls and Holbrook et al. disclose (422) (Figure 6) the formation of a silicon nitride layer (Col. 6, lines 63 – 67) on the walls of the trench. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Holbrook et al. with Lur et al. to provide a liner layer that would reduce sharp edges and roughness of subsequent deposited layers (Col. 6, lines 63 – 67).

Response to Arguments

23. Applicant's arguments in Letter No. 10 of March 18, 2004 have been carefully considered but they have not been found to be persuasive. In particular, Applicant has argued for Claims 1 and 26 that the second dielectric material is "substantially absent" from the wall of the second recessed region. This has been discussed in more detail in the first part of the Office Action and will not be expanded further here.

Applicant has alleged that the thermally grown oxide recited in the instant application is more dense and structurally stronger than the CVD material of the reference. However, there is no recitation in the claim limitations on density and strength requirements for the dielectric layer and the allegation is, hence, not germane. Applicant has also not presented definitive proof that devices made from the oxide in the reference differ substantially from those of the instant application.

Conclusions

24. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee

Steven Loke
Primary Examiner